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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/637,049	08/11/2000	Fan Zhou	FORE-67	7201

7590 11/10/2003

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EXAMINER

MOORE, IAN N

ART UNIT	PAPER NUMBER
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2661

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/637,049

Applicant(s)

ZHOU ET AL.

Examiner

Ian N Moore

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings (Fig. 22 and 23) are objected to under 37 CFR 1.83(a) because they fail to show the “method for switching comprising the steps of: receiving, sending, measuring, appending, storing, reading, and determining” as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. **No new matter should be entered.**

Specification

2. The abstract of the disclosure is objected to because it contains fragment sentences: “A switch for switching packets” (Page 111, line 1) and “A method for switching packets.” (Page 112, line 9). Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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3. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

~~20~~
Claim 3 recites the terms " ... sending with a striper of the port card to the aggregator of each fabric the fragments of the packet" (line 2-3) which renders the claim indefinite. It is unclear what exactly is sending to the aggregator. In particular, the claim recites "...**sending with a striper of the port card...**", which appears to mean that a striper of the port card is being sent along with the fragments to the aggregator, and these terms are particularly unclear with regards to who is sending what or where. Moreover, the claim recites "...**to the aggregator of each fabric fragments of the packets**", which appears to mean that fragments are being sent to each fabric fragments of the packets, and these terms are particularly unclear with regards to who is sending what or where. The claim itself and the specification do not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros (U.S. 5,166,926) in view of Gaddis (U.S. 5,815,501).

Regarding claim 1, Cisneros '926 discloses a switch for switching packets, each packet having a length, comprising:

a port card (see FIG. 3A, Interface Module 210) which receives packets from (see Fig. 3A Incoming User Lines 305) and sends packets to a network (Fig. 3A Outgoing User lines 335; see col. 15, line 44-65, note that each Interface module transmits and receives cells); and

fabrics connected to the port card which switch the packets (see Cisneros '926 Fig. 5, Self-routing cross-point planes 550s connects to Interface Modules 260 and 270; and col. 25, line 63 to col. 26, line 27; Note that Self-routing cross-point planes 550s are “fabrics”).

Cisneros '926 does not explicitly disclose a fabric (see Gaddis '501 FIG. 3, the ATM ATM Ethernet portal Hardware) having a memory mechanism (see Gaddis '501 FIG.3, a combined functionality of Dual-ported Share Memory 24, Control Microprocessor 20, DMA Controller 26 and ATM cell processor), and a fabric having a mechanism for determining the length of each packet (see Gaddis '501 Fig. 5, a length of the arriving Ethernet Frame) received by the fabric and placing a length indicator with the packet (see Gaddis '501 Fig. 5, putting a value in a “SIZE” field in the ATM encapsulation; see col. 8, line 1-17; note that a size field indicates the number of bytes in segment data field. By utilizing the last segment's size field and sequence number, a variable Ethernet frame/packet size is defined.) so when the packet is stored in the memory mechanism, the determining mechanism can identify from the length indicator how long the packet is and where the packet ends in the memory mechanism (see Gaddis '501 col. 9, line 9-46; note the shared memory places the frames into

the memory. Each segment is 44 bytes long, except the last segment. In the shared memory, each 44 byte segments are stored, and the gaps between each segments are padded with inter-cell padding as the placeholders for ATM and SAR headers. Therefore, in order to determine the beginning and the end of each Ethernet frame and being able to insert the placeholders for ATM headers, the shared memory must have a functionality to locate/identify each frame by its size (i.e. the start of the frame or the end of the frame); also see col. 6, line 61-64) .

However, this limitation is taught by Gaddis '501. Cisneros '926 teaches the interface card, which transmits and receives cells and a cross connect plane switch. Gaddis '501 teaches frame segmentation and storing into a shared memory, which locates each frame by the size. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the purpose of dramatically decreasing the processing required by the portal and increasing the data throughput rate. The motivation being that by designing a portal unit switch between Ethernet and ATM system, it will decrease the protocol converting time since the ATM network connection can be setup transparently between Ethernet segments.

Regarding claim 2, Gaddis '501 discloses the determining mechanism includes an aggregator (see Gaddis '501 Fig. 3 Ethernet Controller 22 at the transmission side (i.e. Ethernet to ATM path)) which receives packet fragments from the port card (see Gaddis '501 Fig. 3 Ethernet Controller 22 receiving frame segments from Serial Interface Adapter 22), determines the packet length and appends packet length information to the beginning of the packet in the length indicator (see Gaddis '501 Fig. 5, note that in the ATM encapsulation, a

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“SIZE” field is attached to the header with the value, which indicates the number of bytes in segment data field; also see col. 8, line 1-17, by utilizing the last segment’s size field and sequence number, a variable size Ethernet frame/packet is computed/defined.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 1 above.

Regarding claim 3, Gaddis '501 discloses the memory mechanism includes a memory controller (see Gaddis '501 FIG.3, a combined system of Dual-ported Share Memory 24, the Control Microprocessor 20, ATM cell processor and DMA Controller), the aggregator (see Gaddis '501 Fig. 3 Ethernet Controller 22) sending the packet with the packet length information to the memory controller (see Gaddis '501 col. 5, line 25-33) which stores the packet with the packet length information (see Gaddis '501 col. 5, line 54-60 and col. 9, line 9-46). Note that Ethernet frames with the size/length fields are send from Ethernet Controller to the shared Memory, and the formatted Ethernet frames are stored in the shared memory.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 1 above.

5. Claims 4-6 rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros '926 and Gaddis '501, as applied to claims 1-3 above, and further in view of Joffe (U.S. 6,021,086).

Regarding claim 4, Gaddis '501 discloses that the memory controller has a memory as described in Claim 1-3 above.

Neither Cisneros '926 nor Gaddis '501 explicitly discloses a memory which has a wide cache buffer structure in which multiple packets are put into one word (see Joffe '086 Fig. 5, Shared Memory 26, bits from multiple ports (B1, B2) (i.e. note that multiple ports transmit/receive multiple packets), and Words (W1-Wn); see col. 5, line 46-67; note that one bit from each port is responsible for a single bit position in each word stored in the shared memory. When pluralities of packets arrive at a port, each bit is transferred and stored into each word at the shared memory (i.e. Bit 1 to Bit m storing in each W1 to Wn).)

However, this limitation is taught by Joffe '086. Note that Joffe '086's shared buffer memory has a functionality of storing bits from various packets into a single word.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926 and Gaddis '501, as taught by Joffe '086, for the purpose of designing an improved architecture for providing multiple port access to store multiple packets to a shared memory; see Joffe '086 col. 3, line 1-3. The motivation being that by designing a shared memory buffer which stores each bit from plurality of packets into a single word, it can reduce extra space in the shared buffer memory.

Regarding claim 5, the combined system of Cisneros '926, Gaddis '501, and Joffe '086 discloses that the fabric sends fragments of the packet to the port card as described above in Claim 1-4. Gaddis '501 further discloses the fabric includes a separator (see Gaddis

'501 Fig. 3 Ethernet Controller 22 at the receiving side (i.e. ATM to Ethernet path)) which reads the packets from the memory controller and extracts the packet length information from each packet to determine when each packet ends (see Gaddis '501 Fig. 10; and col. 10, line 1-40; note that when ATM cells arrive from the network, the microprocessor examines each cell to ensure all ATM cells that belongs to an Ethernet frame are received by utilizing the frame size and frame size counter. Once an entire Ethernet frame arrives, Ethernet controller extracts the segments from the shared memory, and then reassembles the Ethernet frame. When the segment is extracted, the size is also extracted from the memory since the size field is in the header of the cells. In order to reassemble Ethernet frame from the ATM cells, the controller must identify where the frame ends.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926 and Gaddis '501 as taught by Joffe '086 for the same reason stated in Claim 4 above.

Regarding claim 6, Cisneros '926 disclose a fabric sending any fragments of each packet to an unstriper of the port card (see FIG. 3A, De-multiplexer 330 of the Interface Module 210 is an "unstriper of the port card"; see col. 16, line 26-48; note that various parts of the cells, from the cross connect plane, are received at the de-multiplexer.) Gaddis '501 discloses that the separator removes the packet length information from each packet before sending any fragments (see Fig. 10; Fig. 5 Ethernet frame and ATM cell, and col. 10, line 31-58; note that each time a new ATM cell is arrived, the size field is updated, which means that the current size of the frame must be deleted first in order to be updated. Once all ATM cells

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that belong to an Ethernet frame arrive, an Ethernet frame is reconstructed as shown in Fig. 5, an Ethernet frame without SIZE field. Thus, it is clear that the size field is deleted after reassembly process at the Ethernet Controller).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926 and Gaddis '501 as taught by Joffe '086 for the same reason stated in Claim 4 above.

6. Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros (U.S. 5,166,926) in view of Gaddis (U.S. 5,815,501).

Regarding claim 7, Cisneros '926 discloses a method for switching packets having a length comprising the steps of:

receiving a packet at a port card of a switch (see FIG. 3A, Interface Module 210 and Incoming User Lines 305; see col. 15, line 44-65, note that each Interface module receives the user packets);

sending fragments of the packet to fabrics of the switch and receiving the fragments of the packet at the fabrics of the switch (see Cisneros '926 Fig. 5, Self-routing cross-point planes 550s connects to Interface Modules 260 and 270; and col. 25, line 63 to col. 26, line 27; Note that the self-routing cross-point planes 550s are "the fabrics of the switch". Since each ATM cell has a fixed size format, it must carry fixed size segments of the variable size user packet. Moreover, the cross-point planes are the switch matrixes, which route the ATM cells to/from the same/different user packet into various paths within the matrix. Thus, the

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segments of the user packet are transmitted/received between the Interface Units and cross connect planes.)

Cisneros '926 does not explicitly disclose measuring the length of the packet at each fabric (see Gaddis '501 FIG. 3, the ATM ATM Ethernet portal Hardware) from the fragments of the packet received at the fabric (see Gaddis '501 col. 7, line 39-48, note that since SAR protocol is used to segment the Ethernet frame, it must first determine the size of the Ethernet frame.);

appending a length indicator to the packet (see Gaddis '501 Fig. 5, putting a value in a "SIZE" field in the ATM encapsulation; see col. 8, line 1-17; note that a size field indicates the number of bytes in segment data field. By utilizing the last segment's size field and sequence number, a variable Ethernet frame/packet size is defined.);

storing the packet with the length indicator in a memory mechanism of the fabric (see Gaddis '501 Fig. 3, the functionality of dual shared memory 24, control microprocessor 20, DMA controller 26 and ATM cell processor is the "memory mechanism"; col. 9, line 9-46; note that the shared memory places the frames into the memory. Each segment is 44 bytes long, except the last segment. In the shared memory, each 44 byte segments are stored, and the gaps between each segments are padded with inter-cell padding as the placeholders for ATM and SAR headers. Therefore, in order to insert the placeholders for ATM headers, the shared memory must have a functionality to determine the beginning and the end of each frame and being able to locate/identify each frame by its size (i.e. the start of the frame or the end of the frame). Also see col. 6, line 61-64);

reading the packet from the memory mechanism (see Gaddis '501 Fig. 9 and col. 10, line 1-40; note that Ethernet Controller reads each segment from the memory in order to reassemble the frame. Also see col. 6, line 61-64); and

determining where the packet ends from the length indicator of the packet (see Gaddis '501 col. 10, line 1-40; note that when ATM cells arrive from the network, the microprocessor examines to ensure all ATM cells, that belong to an Ethernet frame, are received by utilizing the frame size and frame size counter. Once an entire Ethernet frame arrives, Ethernet controller reassembles the Ethernet frame from the segments. In order to reassemble Ethernet frame from the ATM cells, the controller must identify where the frame ends.)

However, this limitation is taught by Gaddis '501. Cisneros '926 teaches the interface card, which receives cells from the network and transmits to the cross connect planes. Gaddis '501 teaches a frame segmentation process that utilizes the size/length of the Ethernet frame to form an ATM cell, storing process that utilizes a shared memory, and re-assembly process that utilizes the size/length of the Ethernet frame. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the purpose of dramatically decreasing the processing required by the portal and increasing the data throughput rate. The motivation being that by designing a portal unit switch between Ethernet and ATM system, it will decrease the protocol converting time since the ATM network connection can be setup transparently between Ethernet segments.

Regarding claim 8, Gaddis '501 discloses the step of receiving the fragment at an aggregator of the fabric (see Gaddis '501 Fig. 3 Ethernet Controller 22 at the transmission side (i.e. Ethernet to ATM path) is the “aggregator”, and it receives Ethernet segments via Serial Interface).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 7 above.

Regarding claim 9, Gaddis '501 discloses the step of measuring the length of the packet with the aggregator (see Gaddis '501 col. 7, line 39-48, note that since SAR protocol is used to segment the Ethernet frame, it must first determine the size of the Ethernet frame. Also, see col. 8, line 1-17, by utilizing the last segment's size field and sequence number, a variable size Ethernet frame/packet is computed/defined.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 7 above.

Regarding claim 10, Gaddis '501 discloses the step of the appending the length indicator to the packet with the aggregator (see Gaddis '501 Fig. 5, note that in the ATM encapsulation, a “SIZE” field is attached to the header with the value, which indicates the number of bytes in segment data field.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 7 above.

Regarding claim 11, Gaddis '501 discloses the step of storing the packet with the length indicator in a memory controller of the memory mechanism (see Gaddis '501 FIG.3, a combined system of Dual-ported Share Memory 24, the Control Microprocessor 20, ATM cell processor, and DMA Controller is “a memory controller”; see col. 5, line 54-60 and col. 9, line 9-46). Note that Ethernet frames with the size fields are send from Ethernet Controller to Shared Memory, and the formatted Ethernet frames are stored in the shared memory.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 7 above.

Regarding claim 12, Gaddis '501 discloses the step of reading the packet from the memory controller with a separator of the fabric (see Gaddis '501 Fig. 3 Ethernet Controller 22 at the receiving side (i.e. ATM to Ethernet path) is “a separator”; also see Gaddis '501 Fig. 9 and col. 10, line 1-40; note that Ethernet Controller reads each segment from the memory in order to reassemble the frame. Also see col. 6, line 61-64).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 7 above.

Regarding claim 13, Gaddis '501 discloses the step of determining where a packet ends from the length indicator with the separator (see Gaddis '501 col. 10, line 1-40; note that when ATM cells arrive from the network, the microprocessor examines to ensure all ATM cells, that belong to an Ethernet frame, are received by utilizing the frame size and frame size counter. Once an entire Ethernet frame arrives, Ethernet controller reassembles the Ethernet frame from the segments. In order to reassemble Ethernet frame from the ATM cells, the controller must identify where the frame ends.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 7 above.

Regarding claim 14, Gaddis '501 discloses the step of removing the packet length information from the separator (see Fig. 10, Fig. 5 Ethernet frame and ATM cell, and col. 10, line 31-58; note that each time a new ATM cells is arrived, the size field is updated, which means that the current size of the frame must be deleted first in order to be updated. Once all ATM cells that belong to an Ethernet frame arrive, an Ethernet frame is reconstructed which as shown in Fig. 5, an Ethernet frame without SIZE field. Thus, it is clear that the size field is deleted after reassembly process at the Ethernet Controller).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 7 above.

Regarding claim 15, Cisneros '926 discloses the step of sending fragments of the packets from cross connect switch to the port card (see FIG. 3A, De-multiplexer 330 of the Interface Module 210; see col. 16, line 26-48; note that various parts of the cells, from the cross connect plane, are received at the interface module 210.) Gaddis '501 discloses the step of sending fragments of the packets from the separator to the interface adaptor (see Fig. 3 Ethernet Controller 22 and Serial Interface Adaptor; Since Ethernet segments are received at Ethernet controller, the same segments must be transmitted from Ethernet Controller to the interface adaptor as well.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926 as taught by Gaddis '501 for the same reason stated in Claim 7 above.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros '926 and Gaddis '501, as applied to claims 7-15 above, and further in view of Jones (U.S. 6,078,595).

Regarding claim 16, the combined system of Cisneros '926 and Gaddis '501 discloses the step of sending fragments of the packet to the port card as described above in Claims 7-15 above. Moreover, Cisneros '926 discloses, as shown in Fig. 5, transmitting and receiving cells between the cross connect planes 550 and Input 260/output 270 Modules.

Neither Cisneros '926 nor Gaddis '501 explicitly discloses the step of sending fragments of the packet in a same logical time with corresponding fragments from other

fabrics (see Jones '595 Fig. 1 Switch Fabrics (SF) 32a and 32b, BITS 14, and Physical Ports 22; see col. 4, line 10-67; note that both switch fabrics are externally timed with BITS (Building Integrated Timing Source) as a primary timing reference. Thus, when transmitting/receiving segments/cells/frames between the switch fabrics to the physical port, it must be synchronized within same clock cycle as primary timing reference.)

However, this limitation is taught by Jones '595. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926 and Gaddis '501, as taught by Jones '595 for the purpose of providing synchronous data transfer within the switch of the present invention, buffering of data communicated between the various switch elements is minimized, reducing system cost, reducing data transfer latency, and enabling alignment of data phase and frequency; see Jones '595 col. 3, line 3-9. The motivation being that by utilizing the reference clock during the transmission of segments/cells/frames, it can minimize the clock slips or timing jitters, which cause failures in the switch and the networks.

8. Claims 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cisneros '926, Gaddis '501 and Jones '595, as applied to claims 7-16 above, and further in view of Joffe '086.

Regarding claim 17, the combined system of Cisneros '926, Gaddis '501 and Jones '595 discloses the step of storing the fragments of the packet in a memory of the memory controller as described in above claims 7-16.

Neither Cisneros '926, Gaddis '501, nor Jones '595 explicitly discloses a memory which has a wide cache buffer structure in which multiple packets are put into one word (see

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Joffe '086 Fig. 5, Shared Memory 26, bits from multiple ports (B1, B2) (i.e. note that multiple ports transmit/receive multiple packets), and Words (W1-Wn); see col. 5, line 46-67; note that each bit from each port is responsible for a single bit position in each word stored in the shared memory. When plurality of packets arrives at a port, each bit is transferred and stored into each word at the shared memory (i.e. Bit 1 to Bit m storing in each W1 to Wn).

However, this limitation is taught by Joffe '086. Joffe '086's shared buffer memory has a functionality of storing bits from various packets into a single word.) Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Cisneros '926, Gaddis '501 and Jones '595, as taught by Joffe '086, for the purpose of designing an improved architecture for providing multiple port access to store multiple packets to a shared memory; see Joffe '086 col. 3, line 1-3. The motivation being that by designing a shared memory buffer which stores each bit from plurality of packets into a single word, it can reduce extra space in the shared buffer memory.

Regarding claim 18, Gaddis '501 discloses the step of extracting the packet length information from the packet with a separator (see Gaddis '501 Fig. 9 and col. 10, line 1-40; note that when ATM cells arrive from the network, the microprocessor examines to ensure all ATM cells, that belong to an Ethernet frame, are received by utilizing the frame size and frame size counter. Ethernet Controller extracts/reads each segment from the memory in order to reassemble the frame. When the segment is extracted/read, the size is also

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extracted/read from the memory since the size field is in the header of the cells. Also see col. 6, line 61-64).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926, Gaddis '501, Jones '595 as taught by Joffe '086 for the same reason stated in Claim 17 above.

Regarding claim 19, Cisneros '926 disclose receiving the fragments of the packet from the fabrics with an unstriper of the port card (see FIG. 3A, De-multiplexer 330 of the Interface Module 210 is an "unstriper".; see col. 16, line 26-48; note that various parts of the cells from the cross connect plane are received at the de-multiplexer.)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926, Gaddis '501, Jones '595 as taught by Joffe '086 for the same reason stated in Claim 17 above.

Regarding claim 20, Gaddis '501 discloses aggregator of each fabric the fragments of the packet as described above in claims 1-19. Furthermore, Cisneros '926 disclose the step of sending with a striper of the port card (see Cisneros '926 FIG. 3A, Multiplexer 320 of the Interface Module 210 is a "striper of the port card".) to each fabric the fragments of packets (see Cisneros '926 col. 15, line 44-65; note that incoming user packets/cells, from the network, are received at the multiplexer.)

Note that Cisneros '926 teaches transmitting segments of user packet from the multiplexer (which is within the interface card) to the cross connect switch plane. Gaddis

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'501 teaches transmitting segments of frame from interface adaptor to the Ethernet Controller (which is within the ATM-Ethernet portal fabric). Thus, Cisneros '926's multiplexer of the interface unit can be used to transmit segments of user packet to Gaddis '501's Ethernet controller which is within the ATM-Ethernet portal fabric. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926, Gaddis '501, Jones '595 as taught by Joffe '086 for the same reason stated in Claim 17 above.

Regarding claim 21, Gaddis '501 discloses the separator sending fragments to the port card as described above in claims 6-20. Cisneros '926 disclose sending fragments from fabrics to an unstriper of the port card (see FIG. 3A, De-multiplexer 330 of the Interface Module 210; see col. 16, line 26-48; note that various parts of the cells, from the cross connect plane, are received at the de-multiplexer.)

Note that Gaddis '501 teaches receiving segments of user packets from the Ethernet Controller to network interface. Cisneros '926 teaches receiving segments of user packets from the cross connect plans to the de-multiplexer (which is within the interface card). Thus, Gaddis '501's Ethernet controller can be used to transmit the segments of the user packets to Cisneros '926's de-multiplexer which is within the interface card. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Cisneros '926, Gaddis '501, Jones '595 as taught by Joffe '086 for the same reason stated in Claim 17 above.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doug Olms can be reached on 703-305-4703. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Ian N Moore
Examiner
Art Unit 2661

INM
11/6/03



KENNETH VANDERPUYE
PRIMARY EXAMINER